

CLAIMS

What is claimed is:

- 1 1. A digital signal processing system that comprises:
2 a shared program memory;
3 a plurality of processor subsystems coupled to the shared program memory to
4 concurrently access instructions stored by the shared program memory,
5 wherein the shared program memory is conditionally write-protected from at least
6 one of the processor subsystems
- 1 2. The system of claim 1, wherein the program memory and the plurality of
2 processor subsystems are fabricated on a single chip.
- 1 3. The system of claim 1, wherein the processor subsystems are prevented from
2 writing anything to the shared program memory while the processor subsystems are in a
3 normal operating mode.
- 1 4. The system of claim 3, wherein the processor subsystems are allowed to write
2 information to the shared program memory while the processor subsystems are in an
3 emulation mode.
- 1 5. The system of claim 1, wherein each of the plurality of processor subsystems
2 includes:
3 a processor core; and
4 an instruction bus that couples the processor core to the shared program memory.
- 1 6. The system of claim 5, wherein each of said processor cores includes a bus
2 interface module coupled to the associated instruction bus to access instructions stored by
3 the shared program memory.

1 7. The system of claim 6, wherein the bus interface module is configured to allow
2 the processor core to perform write operations to the shared program memory only when
3 the processor core is operating in an emulation mode.

1 8. The system of claim 6, wherein the bus interface module is configured to prevent
2 the processor core from writing anything to the shared program memory while the
3 processor core is in a normal operating mode.

1 9. The system of claim 8, wherein the bus interface module is further configured to
2 allow the processor core to write information to the shared program memory while the
3 processor is in an emulation mode.

1 10. The system of claim 9, wherein the bus interface receives a signal that, when
2 asserted, indicates that the processor core is in an emulation mode.

1 11. The system of claim 10, wherein de-assertion of said signal causes said bus
2 interface module to maintain an instruction bus read/write signal in a read state, and
3 wherein assertion of said signal causes said bus interface module to maintain the instruction
4 bus read/write signal in accordance with shared program memory access operations
5 requested by the processor core.

1 12. The system of claim 5, wherein the processor subsystems each further include:
2 data memory coupled to the processor core via a data bus distinct from the
3 instruction bus, wherein the processor core is configured to operate on data
4 from the data memory in accordance with program instruction retrieved via
5 the instruction bus.

1 13. The system of claim 12, wherein the processor subsystems each further include:
2 a direct memory access (DMA) controller; and

3 a memory bus that couples the DMA controller to the data memory and the shared
4 program memory, wherein the memory bus is distinct from the instruction
5 bus and distinct from the data bus.

1 14. The system of claim 5, wherein the program memory is configured to service
2 multiple instruction requests received via the instruction buses in each clock cycle.

1 15. The system of claim 14, wherein the processor cores are configured to
2 concurrently execute distinct instructions from a single program stored in the shared
3 program memory, and wherein the order in which program instructions are executed by a
4 processor core depends on the data that the processor core operates on.

1 16. A method of conditionally write protecting a shared program memory in a
2 multi-core processor chip, wherein the method comprises:
3 receiving a requested shared program memory access operation from a processor
4 core; and
5 combining the requested shared program memory access operation with a signal
6 indicative of a current operating mode to produce a communicated shared
7 program memory access operation, wherein when the current operating
8 mode is a normal operating mode, the communicated shared program
9 memory access operation is prevented from being a write operation.

1 17. The method of claim 16, wherein when the current operating mode is an
2 emulation mode, the communication shared program memory access operation is always
3 the same as the requested shared program memory access operation.

1 18. The method of claim 17, wherein the emulation mode is indicated by the
2 assertion of a suspend signal, and wherein said combining includes:
3 inverting the suspend signal; and

4 performing a logical OR of the inverted suspend signal with a read/write signal
5 included in the requested access operation to produce a read/write signal for
6 inclusion in the communicated access operation.

1 19. A digital signal processor chip that comprises:
2 a volatile memory containing software instructions; and
3 a plurality of processor cores coupled to the volatile memory via a corresponding
4 plurality of instruction buses, wherein the processor cores are configured to
5 retrieve and execute instructions from the volatile memory, and
6 wherein during each of the instruction buses is configured to convey only read
7 operations to the volatile memory while their corresponding processor cores
8 are in a normal operating mode.

1 20. The chip of claim 19, wherein each of the instruction buses includes a
2 read/write signal line that is maintained in a read state while the corresponding processor
3 cores are in the normal operating mode.

1 21. The chip of claim 19, wherein each of the instruction buses is configured to
2 allow both read operations and write operations to be conveyed to the volatile memory
3 while the corresponding processor cores are in an emulation mode.

1 22. The chip of claim 21, wherein each of the instruction buses includes a
2 read/write signal line having a value produced by a logic gate that combines a read/write
3 signal value from the corresponding processor core with an operating mode signal value for
4 the corresponding processor core.

1 23. The chip of claim 22, wherein the operating mode signal acts as a gate control
2 signal that prevents the read/write signal from the corresponding processor core from
3 affecting the read/write signal on the instruction bus.

1 24. The chip of claim 22, further comprising:
2 a test port; and
3 emulation logic that provides determines the operating mode signals for each of the
4 processor cores in response to control information received via the test port.

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